

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,761,683 B2
APPLICATION NO. : 10/091698
DATED : July 20, 2010
INVENTOR(S) : Brian N. Ripley

Page 1 of 3

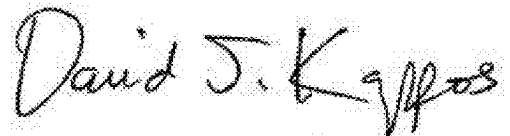
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Delete the title sheet showing an illustrative figure and substitute the attached title page therefor.

Delete sheet 3 of 6 in figure 3A, and substitute the attached sheet 3.

On Sheet 5 of 6, in figure 4, add element "400", above Figure.

Signed and Sealed this
Eighth Day of November, 2011

A handwritten signature in black ink, reading "David J. Kappos". The signature is written in a cursive, flowing style with a large initial "D".

David J. Kappos
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Ripley

(10) **Patent No.:** **US 7,761,683 B2**
(45) **Date of Patent:** **Jul. 20, 2010**

(54) **VARIABLE WIDTH MEMORY SYSTEM AND METHOD**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 819 days.

(21) Appl. No.: **10/091,698**

(22) Filed: **Mar. 5, 2002**

(65) **Prior Publication Data**
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(51) **Int. Cl.**
G06F 12/02 (2006.01)
G06F 12/04 (2006.01)

(52) **U.S. Cl.** **711/170; 711/171; 711/172; 711/173; 711/202; 711/212**

(58) **Field of Classification Search** **711/202, 711/170, 171, 172, 173, 212**
See application file for complete search history.

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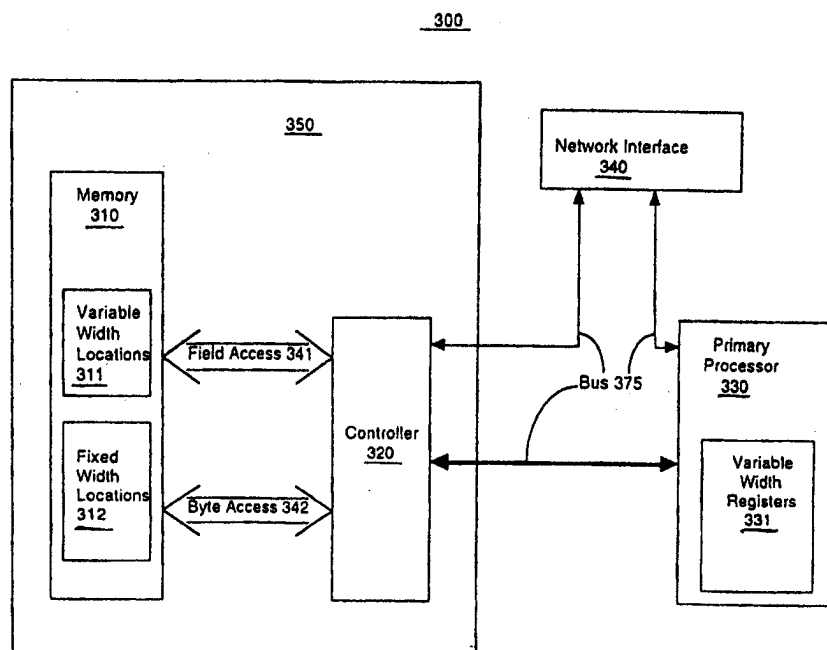
* cited by examiner

Primary Examiner—Sanjiv Shah
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(57) **ABSTRACT**

A variable width memory system is disclosed. The variable width memory system facilitates efficient utilization of memory resources and delivery of information in a convenient manner. A plurality of memory locations store information and the bit widths of at least two of the memory locations are different. A controller directs access to the plurality of memory locations. Information is communicated between the controller and memory locations via a bus coupled to the controller and memory locations.

22 Claims, 6 Drawing Sheets



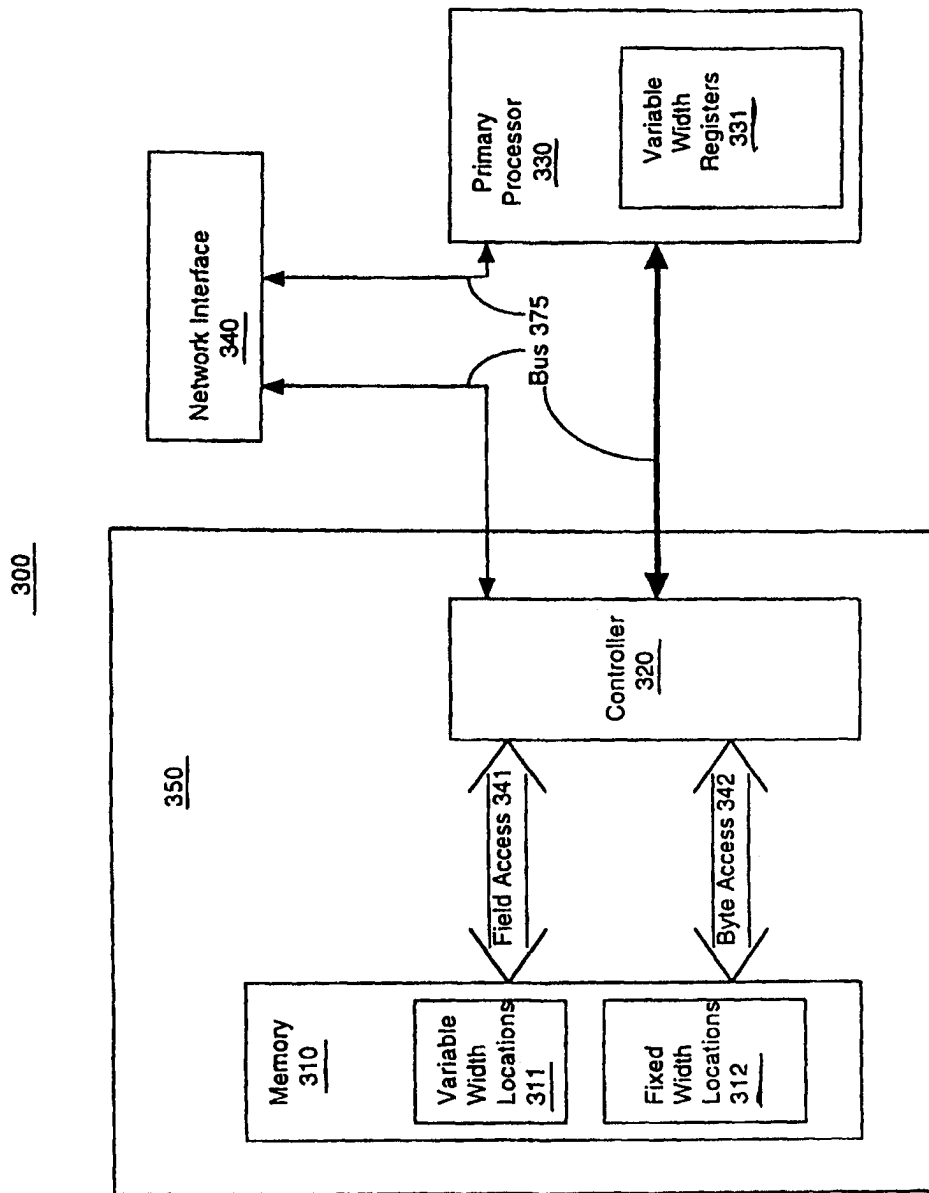


FIG 3A